REMARKS

I. Introduction

Claims 1-14 are pending in this application, of which claims 1 and 10 are independent. In this Amendment, claims 1, 4, and 10 have been amended. Care has been exercised to avoid introduction of new matter. Support for the amendment of the claims can be found in, for example, Fig. 1 and relevant description of the specification.

A Substitute Specification to amend the written description of the specification has also been submitted concurrently with this Amendment.

II. The Objection to the Specification

The Examiner suggested replacing the term "shift resister" in the specification with --shift register--. In response, the Substitute Specification has been submitted to correct the typographic oversights. The abstract of the disclosure has also been amended. Withdrawal of the objection to the specification is, therefore, respectfully solicited.

III. The Objection to Claim 4

Objection has been made to claim 4 because the term "shift resistor" should be replaced with --shift register--. Claim 4 has been amended in the manner suggested by the Examiner. Applicant, therefore, respectively solicits withdrawal of the objection to claim 4.

IV. The Rejection of Claims 1-5, 10, and 11

Claims 1-5, 10, and 11 have been rejected under 35 U.S.C. §102(a) as being anticipated by Kurosawa et al. The Examiner asserted that a MOS-based image sensor identically corresponding to what is claimed.

Applicant submits that Kurosawa et al. does not identically disclose a solid-state imaging apparatus including all the limitations recited in independent claim 1. Specifically, the reference does not disclose, at a minimum, "the drive circuit region includes at least a vertical shift register and a horizontal shift register, and all the transistors in the imaging region and the drive circuit region have a same channel polarity," recited in claim 1. In a solid-state imaging apparatus of claim 1, the drive circuit region includes at least a vertical shift register and a horizontal shift register. All the transistors in the imaging region and the drive circuit region (which includes at least a vertical shift register and a horizontal shift register) have the same channel polarity.

Kurosawa et al. in Figs. 4 and 12 discloses a CMOS-type solid-state imaging apparatus (see paragraph [0002]) having an imaging region (effective pixel array) 11 and a driving circuit region. Imaging region 11 includes a plurality of amplification-type unit pixels 180. Each unit pixel 180 includes a photodiode and an amplifier unit that amplifies a signal charge generated by the photodiode. The drive circuit region includes vertical shift register (vertical scanning circuit) 13, horizontal shift register (horizontal scanning circuit) 14, readout circuit 15, signal level adjusting circuit 17, and black-level signal generation circuit 21. Readout circuit 15 includes a plurality of readout portions 260.

In Kurosawa et al., all of the transistors of unit pixels 180 included in imaging region 11 and those of readout portions 260 included in readout circuit 15 have the same channel polarity (N-ch). However, Kurosawa et al. does not disclose that the transistors of the other circuits in

the drive circuit region, such as vertical shift register 13 and horizontal shift register 14, have the same channel polarity as that of the readout portions 260 and so on. Since Kurosawa et al. is directed to a CMOS-type solid-state imaging apparatus, it is apparent that transistors have different channel polarities unless otherwise indicated. That is, both p-channel transistors and n-channel transistors exist in the apparatus of Kurosawa et al.

In contrast, claim 1 recites that all the transistors in the imaging region and the drive circuit region (including at least a vertical shift register and a horizontal shift register) have the same channel polarity. Accordingly, the number of processes required for forming all the transistors in both regions is only approximate one half the number of processes required for manufacturing the conventional solid-state imaging apparatus with the use of the CMOS processing technology. This means that the imaging region suffers less damage during the process for forming the transistors. Therefore, the solid-state imaging apparatus suffers less damage in the imaging region during the manufacturing process, and suffers less noise in the application unit and less leakage current in the photodiode unit. As a result, the solid-state imaging apparatus can realize a high image quality. Kurosawa et al. is silent on the claimed limitation and the above described benefits.

Based on the foregoing, Kurosawa et al. does not identically disclose a solid-state imaging apparatus including all the limitations recited in independent claim 1. The above discussion is also applicable to independent claim 10 reciting a manufacturing method for a solid-state imaging apparatus. Claim 10 recites, "all transistors formed in both steps for forming the imaging region and the drive circuit region respectively are MOS type transistors having a same channel polarity" (the drive circuit region includes at least a vertical shift register and a horizontal shift register). Dependent claims 2-5 and 11 are also patentably distinguishable over

Kurosawa et al. at least because these claims include all the limitations recited in independent claims 1 and 10. Applicant, therefore, respectfully solicits withdrawal of the rejection of the claims under 35 U.S.C. §102(a) and favorable consideration thereof.

V. The Rejection of Claims 6-9 and 12-14

Claims 6-8 and 12-14 have been rejected under 35 U.S.C. §103(c) as being unpatentable over Kurosawa et al. in view of Momose et al.; and claim 9 has been rejected under 35 U.S.C. §103(c) as being unpatentable over Kurosawa et al. in view of Shinohara et al.

Claims 6-9 and 12-14 depend from independent claims 1 and 10, respectively. Applicant, thus, incorporates herein the arguments previously advanced in responding to the rejection of claims 1 and 10 under 35 U.S.C. §102 for anticipation evidenced by Kurosawa et al. The Examiner's additional comments and secondary reference to Momose et al. and Shinohara et al. do not cure the previously argued deficiencies of Kurosawa et al. Applicant, therefore, respectfully solicits withdrawal of the rejection of the claims and favorable consideration thereof.

VI. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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